AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-10. (Cancelled)

11. (currently amended) A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs,

wherein each ~~of the~~ match line ~~pairs~~ pair has a precharge circuit associated therewith, [[;]] the precharge circuit ~~drives the~~ driving a first match line of the match line pair to ~~the~~ a first voltage and ~~the~~ driving a second match line ~~thereof~~ of the match line pair to ~~the~~ a second voltage lower than the first voltage, ~~respectively;~~

wherein each of the memory cells has a storage circuit and a comparator circuit, [[;]]

wherein each ~~of the comparators~~ comparator circuit has ~~the~~ a first MOS transistor and ~~the~~ a second MOS ~~transistors;~~transistor, with a gate ~~electrodes~~ electrode of

the first MOS transistor being connected to a first search line of the associated search line pair and with a gate electrode of the second MOS ~~transistors are~~ transistor being connected to ~~the~~ a second search ~~lines, respectively;~~ line of the associated search line pair,

wherein, for each of the first MOS transistor and the second MOS transistor, ~~either~~ one of a source electrode ~~or~~ and a drain ~~electrodes~~ electrode ~~of the first and second MOS transistors are~~ is connected to the associated first match line, [[;]] and

wherein ~~the~~ each second match line is put in a floating state when the associated comparator circuit performs a comparison operation. ~~is performed in the comparator.~~

12. (currently amended) The semiconductor integrated circuit device according to claim 11,

wherein a source - drain path in ~~the~~ each first MOS transistor is included in ~~the~~ a first current path between the associated first and the second match lines, [[;]]

wherein a source - drain path in ~~the~~ each second MOS transistor is included in ~~the~~ a second current path between the associated first and the second match lines, [[;]] and

wherein ~~the~~ each comparator circuit generates a signal voltage corresponding to a result of comparing data stored

~~at~~ in the storage circuit ~~and~~ with data inputted via the search lines at ~~the~~ an associated one of the first match line and the second match line.

13. (currently amended) The semiconductor integrated circuit device according to claim 12, wherein ~~the~~ first and ~~the~~ second parasitic coupling capacitances ~~being parasitic~~ between ~~the~~ respective search ~~line~~ lines of a search line pair and the associated first match line are larger than ~~the~~ third and ~~the~~ fourth parasitic coupling capacitances ~~being parasitic~~ between the respective search ~~line~~ lines and the associated second match line.

14. (currently amended) The semiconductor integrated circuit device according to claim 13,

wherein a match detector is ~~arranged in~~ coupled to each of the second match lines, [[;]] and

wherein the match detector determines the ~~data-comparison~~ data-comparing result by discriminating voltages of the second match line coupled thereto.

15. (currently amended) The semiconductor integrated circuit device according to claim 14, wherein each ~~the~~ storage circuit has two transistors and two capacitors.

16. (currently amended) A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs,

wherein ~~the~~ each match line pair has a precharge circuit associated therewith, [[;]] the precharge circuit ~~drives the~~ driving a first match line of the match line pair to ~~the~~ a first voltage and ~~the~~ driving a second match line ~~thereof~~ of the match line pair to ~~the~~ a second voltage lower than the first voltage, ~~respectively;~~

wherein ~~the~~ each memory cell has a storage circuit and a comparator circuit, [[;]]

wherein ~~the~~ each comparator circuit comprises:

~~the~~ a first MOS transistor and ~~the~~ a second MOS ~~transistors~~ transistor connected serially ~~so as~~ to form ~~the~~ a first current path between ~~the~~ associated ones of the first and the second match lines, and

~~the~~ a third MOS transistor and ~~the~~ a fourth MOS ~~transistors~~ transistor connected serially ~~so as~~ to form ~~the~~ a second current path, [[;]]

wherein gate electrodes of the first and third MOS transistors are respectively connected to ~~the~~ a first search line and a second search line of the associated search ~~lines~~ line pair, ~~respectively;~~

wherein, for each of the first MOS transistor and the third MOS transistor, one of a source electrode and a drain electrode is connected to the associated first match line through a first contact having a lower surface contacting said one source and drain electrode and an upper surface contacted with the first match line,

~~either of electrodes of source or drain electrodes of the first and the third MOS transistors are connected to the first match lines through contacts formed through self-aligned process;~~

wherein gate electrodes of the second and fourth MOS transistors are connected to the associated storage circuit, ~~circuits, respectively;~~ and

~~either of electrodes~~ wherein, for each of the second MOS transistor and the fourth MOS transistor, one of a source electrode ~~or~~ and a drain ~~electrodes~~ electrode ~~of the second and fourth MOS transistors are~~ is connected to the associated second match line ~~lines~~ through a second contact having a lower surface contacting said one source and drain electrode and an upper surface contacting the associated

second match line, ~~contacts formed through self aligning process.~~

wherein the lower surface of the first contact is smaller than the upper surface of the first contact, and

wherein the lower surface of the second contact is smaller than the upper surface of the second contact.

17. (currently amended) The semiconductor integrated circuit device according to claim 16,

wherein ~~the~~ first and ~~the~~ second parasitic coupling capacitances ~~being parasitic~~ between ~~the~~ respective search lines of a search line pair and the associated first match ~~lines~~ line are generated ~~principally~~ by an interlayer insulator formed between the first contact and the respective gate electrodes of the associated first and third MOS transistors, ~~the contacts, respectively;~~

wherein ~~the~~ third and ~~the~~ fourth parasitic coupling capacitances ~~being parasitic~~ between ~~the~~ respective search lines of the search line pair and the associated second match ~~lines~~ line are generated ~~principally~~ by an interlayer insulator formed between a first metal layer used ~~for forming~~ to form the plurality of ~~the~~ search line pairs and a second metal layer used ~~for forming~~ to form the plurality of ~~the~~ second match lines, [[;]] and

wherein the first and the second parasitic coupling capacitances are larger than the third and the fourth parasitic coupling capacitances, respectively.

18. (currently amended) A semiconductor integrated circuit device comprising a plurality of the first match lines, a plurality of search line pairs intersecting the plurality of ~~the~~ first match lines, a plurality of bit line pairs ~~paralleling~~ arranged parallel to the plurality of search line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of ~~the~~ first match lines with the plurality of search line pairs,

wherein ~~the~~ each memory cell has a storage circuit and a comparator circuit, [[;]]the storage circuit ~~is~~ being connected to an associated one of the bit line pairs, [[;]] and the comparator circuit being ~~is~~ connected to an associated one of the search line pairs and an associated one of the first match lines, [[;]]

wherein a voltage supplied to the plurality of bit lines pairs varies between a first voltage and a second voltage lower than the first voltage,

~~the~~ wherein a voltage supplied to ~~amplitude of~~ the plurality of search line pairs varies between a third voltage and a fourth voltage lower than the third voltage,

wherein the first voltage is larger than the third voltage,

~~bit line pairs is larger than that of the plurality of search line pairs;~~

wherein a plurality of second match lines are arranged parallel to the plurality of first match lines, ~~are provided;~~

wherein a plurality of match line pairs are formed ~~in a paired manner~~ by associated ones of the plurality of first match lines and associated ones of the plurality of second match lines, each match line pair having ~~have~~ respective precharge circuits associated therewith, the ~~plurality of~~ precharge circuits ~~drive~~ driving the associated first match line ~~lines of the match line pairs~~ to ~~a~~ the first voltage and driving the associated second match line ~~lines of the match line pairs~~ to ~~a~~ the second voltage, ~~lower than the first voltage, respectively,~~ and each ~~the~~ comparator circuit ~~is inserted~~ being arranged between ~~the plurality of~~ an associated match line ~~pairs~~ pair to compare data held ~~at~~ in the associated storage circuit ~~and~~ with data inputted via ~~the plurality of~~ associated search lines of a search line pair, [[;]] and

wherein ~~the~~ each second match line is put in a floating state at a time of comparison operation in the associated comparator.

19. (previously presented) The semiconductor integrated circuit device according to claim 18, wherein each of the storage circuits has two transistors and two capacitors.

20. (new) The semiconductor integrated circuit device according to claim 16, wherein the second voltage and the fourth voltage are the same.